Amendments to the Specification:

On page 3, please replace the paragraph beginning at line 8 with the following amended paragraph:

Figure 1 depicts a block diagram of an exemplary inverter controller integrated circuit 10 according to the present invention. In this exemplary embodiment, the controller 10 is an 8 pin design (labeled 1-8), where pin 2 is adapted to receive two signals and multiplexed to support two functions, and pin 4 is adapted to receive two signals to support two functions, depending on the state of certain components of the controller. In this example, pin 2 supports both load voltage sensing and dim signal sensing. Pin 4 supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

On page 5, please replace the paragraph beginning at line 16 with the following amended paragraph:

Dimming circuitry 200 is enabled by the MUX circuit 18 (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN 2). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry 200 is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal 50) ~~that its~~ that's duty cycle is proportional to Vdim. The frequency of the burst mode signal 50 is

selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35-80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

On page 6, please replace the paragraph beginning at line 5 with the following amended paragraph:

In the exemplary embodiment, dimming circuit 200 comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit 36 generates a burst mode signal 50 that has a duty cycle ~~proprtial~~ proportional to the value of Vdim. In this example, the duty cycle of the burst mode signal 50 ranges from 0% (Vdim=V1) to 100% (Vdim=V2).

On page 8, please replace the paragraph beginning at line 13 with the following amended paragraph:

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit 74 is set), the current sense value Isens stays below the lamp threshold signal 46, the output of the amplifier 28 changes the state of the lamp on signal 34. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit 100 to PIN 2. As is understood in the CCFL arts, Vsens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however, and open or broken lamp condition

exists, Vsens will rise to a value greater than V2. When PIN 2 is coupled to the overvoltage protection circuit 100, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in comparator 22. When Vsens exceeds Vovp 48, the output of comparator causes timing circuit 24 to initiate[[s]] a predefined timeout period.

On page 9, please replace the paragraph beginning at line 3 with the following amended paragraph:

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal 46. Also, error amplifier 30 will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the ~~timout~~ timeout period, the protection circuit operates in a manner similar to the PWM enable circuit 38. During this period, to prevent the error amplifier from generating a error ~~singal~~ signal to cause the switches to drive at higher power, the OVP signal 60 stops the error amplifier 30 to charge/discharge of CMP capacitor 40. At the end of the timout, the protection circuit 26 disables the switch driver logic 44 and thus the output overvoltage is controlled.

On page 9, please replace the paragraph beginning at line 12 with the following amended paragraph:

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit 100 configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit 200 configured to receive a dimming signal

and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit 300 configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit 400 configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN 2) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer 18 is coupled to the pin and configured to direct the voltage feedback signal to the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

On page 11, please replace the paragraph beginning at line 18 with the following amended paragraph:

The controller 10' also includes a min/max circuit 56 which, during times when the burst mode signal is enabled, generates a minimum DC value (instead of a zero DC value 52, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the min/max circuit 56 generates an output to cause the output signals to have some predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintains continuous function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

On page 13, please replace the paragraph beginning at line 3 with the following amended paragraph:

Thus, the exemplary inverter controller ICs 10 and 10' of Figures 1 and 2 include a pin (e.g., PIN2) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverter controller ICs 10 and 10' are also adapted to include a pin (e.g., PIN 4) that is multifunctional to operate ~~is~~ in a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

On page 14, please replace the paragraph beginning at line 21 with the following amended paragraph:

Still other modifications may be made. For example, the exemplary application topologies of Figures 3 and 4 depict the controller ICs 10 or 10' driving a derived Royer circuit formed by Q1 and Q. However, the controller 10 or 10' may be likewise applied to a push-pull inverter, a half bridge inverter and/or [[or]] other type of two switch inverter topology known in the art. Yet further, the controller IC 10 or 10' may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC 10 or 10' to drive a four switch inverter topology (e.g., full bridge inverter).

On page 15, please replace the paragraph beginning at line 5 with the following amended paragraph:

The present invention is not limited to a CCFL load. Indeed the controller 10 or 10' of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller 10 or 10' of the present

invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the load type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in Figure 4, numerous other topologies may be used, for example as described in U.S. Patent No. 6,104,146, and U.S. Patent Application Serial Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are ~~encorporated~~ incorporated by reference in their entirety.